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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/587,604	07/27/2006	Petrus Maria De Greef	NL040106US1	3561

65913 7590 06/23/2008

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EXAMINER	
MARTELLO, EDWARD	

ART UNIT	PAPER NUMBER
2628	

NOTIFICATION DATE	DELIVERY MODE
06/23/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/587,604	DE GREEF, PETRUS MARIA	
	Examiner	Art Unit	
	Edward Martello	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 July 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7/27/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Amended claims 1-11, dated 07/27/2006, are pending in this application.

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference characters "2" and "32+34+35" are used to designate the same function in figures 1 and 2 respectively. Likewise, the display driver block of figure 1, reference number 3, is expanded in figure 2 to reference designators 30+31+32. In both cases, no highlighting such as boxing in or dashed lines around the expanded functional blocks is provided and there is no reference designation of 2 or 3 in figure 2 which would tie the two drawings together. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-4 and 6-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Schiefer et al. (European Patent Application Publication EP 0 875 882 A2, hereafter, '882).

4. Regarding claim 1, Schiefer teaches a display method comprising generating images comprising source data (input video; '882; fig. 1 & 2; col. 10, ln. 14-26) and source frame (vertical) synchronization instants (IPVSYNC) shaving a source frame rate, storing the source data in a frame memory (memory, '882; fig. 3; col. 11, ln. 51-58) under control of a first address pointer (write counter) having a start address being determined by the source frame synchronization instants (IPVSYNC) ('882; col. 13, ln. 13-39), reading during a read period, display data from the memory under control of a second address pointer having a start address being determined by display frame synchronization instants (DVSYNC) having a display frame rate ('882; col. 14, ln. 5-35), displaying the display data on a matrix display ('882; fig. 2) and controlling the source frame rate or the display frame rate to obtain, in a stable situation (display synchronizer; '882; col. 17, ln. 50-58, col. 18, ln. 1-10), the first address pointer and the second address pointer starting with an offset in time which has a fixed polarity during the read period ('882; col. 17, ln. 12-20) and a ratio of two between the display frame rate and the source frame rate ("882; fig. 11-15, DCLK = 2*IPCLK, col. 21, ln. 15-20).

5. In regards to claim 2, Schiefer teaches a display system comprising a video source for generating images comprising source data (input video; '882; fig. 1 & 2; col. 10, ln. 14-26) and source frame (vertical) synchronization instants (IPVSYNC) having a source frame rate, means for storing the source data in a frame memory (memory, '882; fig. 3; col. 11, ln. 51-58) under control of a first address pointer (write counter) having a start address being determined by the source frame synchronization instants (IPVSYNC) ('882; col. 13, ln. 13-39); means for reading

during a read period display data from the memory under control of a second address pointer (read counter) having a start address being determined by display frame synchronization instants (DVSYNC) having a display frame rate ('882; col. 14, ln. 5-35), means for displaying the display data on a matrix display ('882; fig. 2) and means for controlling the source frame rate or the display frame rate to obtain, in a stable situation (display synchronizer; '882; col. 17, ln. 50-58, col. 18, ln. 1-10), the first address pointer and the second address pointer starting with an offset in time which has a fixed polarity during the read period ('882; col. 17, ln. 12-20) and a ratio of two between the display frame rate and the source frame rate ("882; fig. 11-15, DCLK = 2*IPCLK, col. 21, ln. 15-20).

6. Regarding claim 3, Schiefer further teaches a display system wherein the means for controlling comprise: means for comparing the source frame synchronization instants (IPVSYNC) and the display synchronization instants (DVSYNC) or signals related thereto ('882; fig. 13; col. 21, ln. 15-34), and means for adapting the source frame rate or the display frame rate in response to the comparing to obtain the second pointer always lagging ("882; fig. 13, DTGRUN signal) the first pointer during the read period in times or the other way around ('882; fig. 13; col. 21, ln. 15-34).

7. Regarding claim 4, Schiefer further teaches a display system wherein the means for controlling comprise: means for determining the offset in time between one of the source frame synchronization instants (IPVSYNC) and one of the display frame synchronization instants (DVSYNC) succeeding each other("882; col. 21, ln. 34-46), and means for adapting the source frame rate or the display frame rate to obtain a substantially identical source frame rate and

display frame rate ('882; col. 21, ln. 34-46); and a predetermined fixed value of the offset in time ('882; fig. 13, DTGRUN signal).

8. In regards to claim 6, Schiefer further teaches a display system as claimed in claim 2, wherein the means for displaying the display data further comprise: means for generating a clock signal (DCLK; '882; fig.7), and means for generating the display frame synchronization instants using the clock signal (DVSYNC; '882, fig. 10); and wherein the means for controlling the display frame rate comprise means for adapting a frequency of the clock signal ('882; col. 15, ln. 29-37; col. 20, ln. 9-14).

9. Regarding claim 7, Schiefer further teaches a display system wherein the means for displaying the display data further comprise: means for generating a clock signal (DCLK; '882; fig.7), means for generating line instants indicating a start of the lines of the display data using the clock signal (DHSYNC; '882; fig. 9), the line instants (DHSYNC) determining line periods, and means for generating the display frame synchronization instants (DVSYNC) using the line instants (DHSYNC) ('882; col. 21, ln. 23-28), and wherein the means for controlling the display frame rate comprise means for adapting a frequency of the clock signal to vary a duration of the line periods ('882; col. 15, ln. 29-37; col. 20, ln. 9-14).

10. In regards to claim 8, Schiefer further teaches a display system wherein the means for displaying the display data further comprise: means for generating a clock signal (DCLK; '882; fig.7), means for generating line instants indicating a start of the lines of the display data by counting the clock signal (DHSYNC; '882; fig. 9), the line instants determining line periods, and means for generating the display frame synchronization instants (DVSYNC) using the line instants ('882; col. 21, ln. 23-28), and wherein the means for controlling the display frame rate

comprise means for adapting the line periods by varying a number of clock pulses of the clock signal to be counted ('882; col. 22, ln. 9-35).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

11. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schiefer et al. (European Patent Application Publication EP 0 875 882 A2, hereafter, '882).

12. Regarding claim 5, Schiefer teaches a display system as claimed in claim 4 but does not teach wherein the means for adapting are arranged to obtain the offset in time between the first pointer and the second pointer being substantially equal to half a source write period, the source write period being the period in time required for the storing of the source data of one source frame of the source data. It would have been obvious to one of ordinary skill in the art at the time of the invention to provide the means for adapting are arranged to obtain the offset in time between the first pointer and the second pointer being substantially equal to half a source write

period, the source write period being the period in time required for the storing of the source data of one source frame of the source data for the benefit of maintaining the optimum buffer fill to allow the most overrun and under run protection to handle short term variations is input video and output display timing that may occur in any system operating over a range of environmental conditions such a temperature, voltage, etc.

13. Claims 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schiefer et al. (European Patent Application Publication EP 0 875 882 A2, hereafter, '882) as applied to claims 1-8 above, and further in view of Chen et al. (U. S. Patent Application 2003/0164897 A1, hereafter '897).

14. Regarding claim 9, Schiefer teaches a display system method as claimed in claim 2 but does not teach wherein a display frame period has a duration being an inverse of the display frame rate and comprises the means for read period and an idle period, wherein during the read period, the means for reading are arranged for reading the display data from the memory under control of the second address pointer, and wherein during the idle period no display data is read from the memory and wherein the means for controlling the display frame rate comprises means for varying the idle time. Chen, working in the same field of endeavor, however, teaches wherein a display frame period has a duration being an inverse of the display frame rate and comprises the means for read period and an idle period (current line delay), wherein during the read period, the means for reading are arranged for reading the display data from the memory under control of the second address pointer (output x & y counters), and wherein during the idle period (current line delay) no display data is read from the memory (outputs blank lines) and wherein the means for controlling the display frame rate comprises means for varying the idle

time ('897; fig. 7; ¶ 0124) for the benefit of synchronizing video image input and display image output frame rates without adjusting either the input or output video clock frequencies thereby simplifying overall clock circuit design and lowering cost. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Schidfer and Chen to produce a method that controls the output video idle period to synchronize the video output frame rate to the video input frame rate with the benefit of not adjusting either of the input or output video clock frequencies thus simplifying overall clock circuit design and lowering cost.

15. In regards to claim 10, Chen further teaches wherein the means for controlling comprise: means for determining the offset in time, and means for adapting the display frame rate to obtain a display frame rate being substantially identical to two times the source frame rate and to obtain a predetermined fixed offset in time, by having (i) the second pointer (output x & y counters) pointing to a first source video line of an already stored source video frame at an instant preceding the instant the first pointer (input x & y counters) is pointing to a first source video line a next source video frame to read the first source video line before the first source video line of the next source video frame is stored, and (ii) the second pointer (output x & y counters) pointing to a last source video line of the next source video frame at an instant later than an instant the first pointer (input x & y counters) is pointing to the last source video line of the next source video frame to read the last source video line of the next source video frame after it has been stored ('897; fig. 8-9, ¶ 0127-0128).

16. Regarding claim 11, Chen further teaches a display system wherein a display frame period has a duration being an inverse of the display frame rate and comprises the read period and an idle period, wherein during the read period, the means for reading are arranged for

reading the display data from the memory under control of the second address pointer (output x & y counters), and wherein during the idle period no display data is read from the memory (outputs blank lines) and wherein the means for controlling comprise: means for setting a free running display frame rate to a value lower than the value of the source display frame rate wherein a duration of the read period is shorter than a source frame period ('897; ¶ 0115), and means for restarting the display frame periods in response to received source (input vertical) synchronization instants ('897; fig. 3, ¶ 0117).

Conclusion

The following prior art, made of record, was not relied upon but is considered pertinent to applicant's disclosure:

US 20030184678 A1	Display controller provided with dynamic output clock
US 6661427 B1	Graphics display system with video scaler
US 6028586 A	Method and apparatus for detecting image update rate differences

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Edward Martello whose telephone number is (571) 270-1883. The examiner can normally be reached on M-F 7:30-5:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Xiao Wu can be reached on (571) 272-7761. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/EM/

Examiner, Art Unit 2628

/XIAO M. WU/

Supervisory Patent Examiner, Art Unit 2628